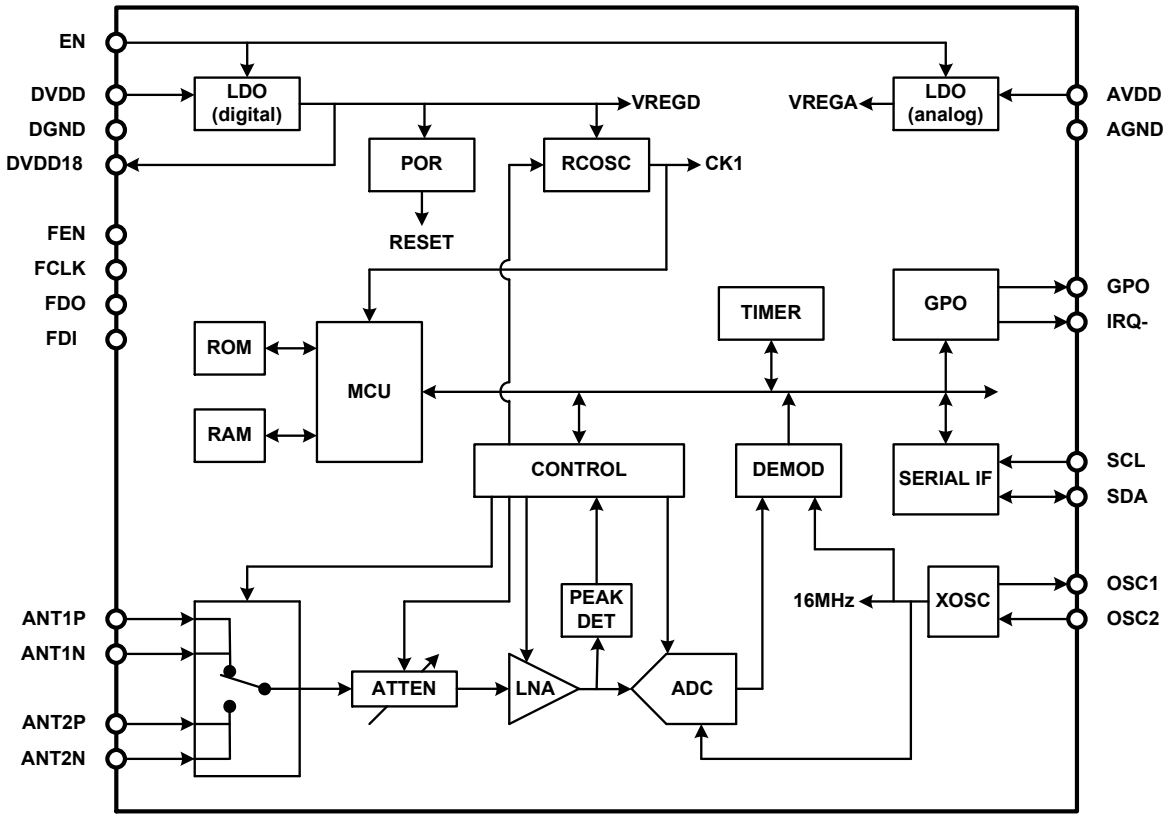
EverSet™ WWVB Receiver – ES100

GENERAL DESCRIPTION

The ES100 is a fully self-contained phase modulation time code receiver that receives and decodes the 60 kHz time signal from the National Institute of Standards and Technology's WWVB transmitter located in Ft. Collins, Colorado, USA. It contains a digital correlation receiver to extract the time code information from the received signal. It also has a simple serial interface to transfer the date, time, and DST information to a host microcontroller. The ES100 is compatible with existing WWVB receive antennas and offers significantly improved performance in low signal-to-noise and low signal-to-interference scenarios when compared to amplitude modulation receivers.

FEATURES	APPLICATIONS
• Receives new phase-modulated WWVB signal • Significantly outperforms all other WWVB receivers • Low power dissipation • 2-wire serial interface • Two antenna inputs	• Analog and digital wall clocks • Clock radios • Consumer Electronics

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Name	Description	Type	Input/ Output
AVDD	Power Supply - Analog	power	-
AGND	Ground - Analog	power	-
DVDD	Power Supply – Digital	power	-
DGND	Ground - Digital	power	-
ANT1P	First Antenna Input, positive	analog	I
ANT1N	First Antenna Input, negative	analog	I
ANT2P	Second Antenna Input, positive	analog	I
ANT2N	Second Antenna Input, negative	analog	I
DVDD18	Digital Voltage Regulator Output.	analog	O
OSC1	16 MHz Crystal Oscillator Output.	analog	O
OSC2	16 MHz Crystal Oscillator Input.	analog	I
EN	Enable Input. When low, the ES100 powers down all circuitry. When high, the device is operational.	digital	I
SCL	Serial Interface Clock.	digital	I
SDA	Serial Interface Data.	digital	I/O
GPO	Connect to a test point on the PCB.	digital	O
IRQ-	Interrupt Output. Active low to signal data available to an external controller.	digital	O
FCLK	Used for IC testing only. This pin must be unconnected on the PCB.	digital	O
FDI	Used for IC testing only. This pin must be unconnected on the PCB.	digital	I
FDO	Used for IC testing only. This pin must be unconnected on the PCB.	digital	O
FEN	Used for IC testing only. This pin must be unconnected on the PCB.	digital	O

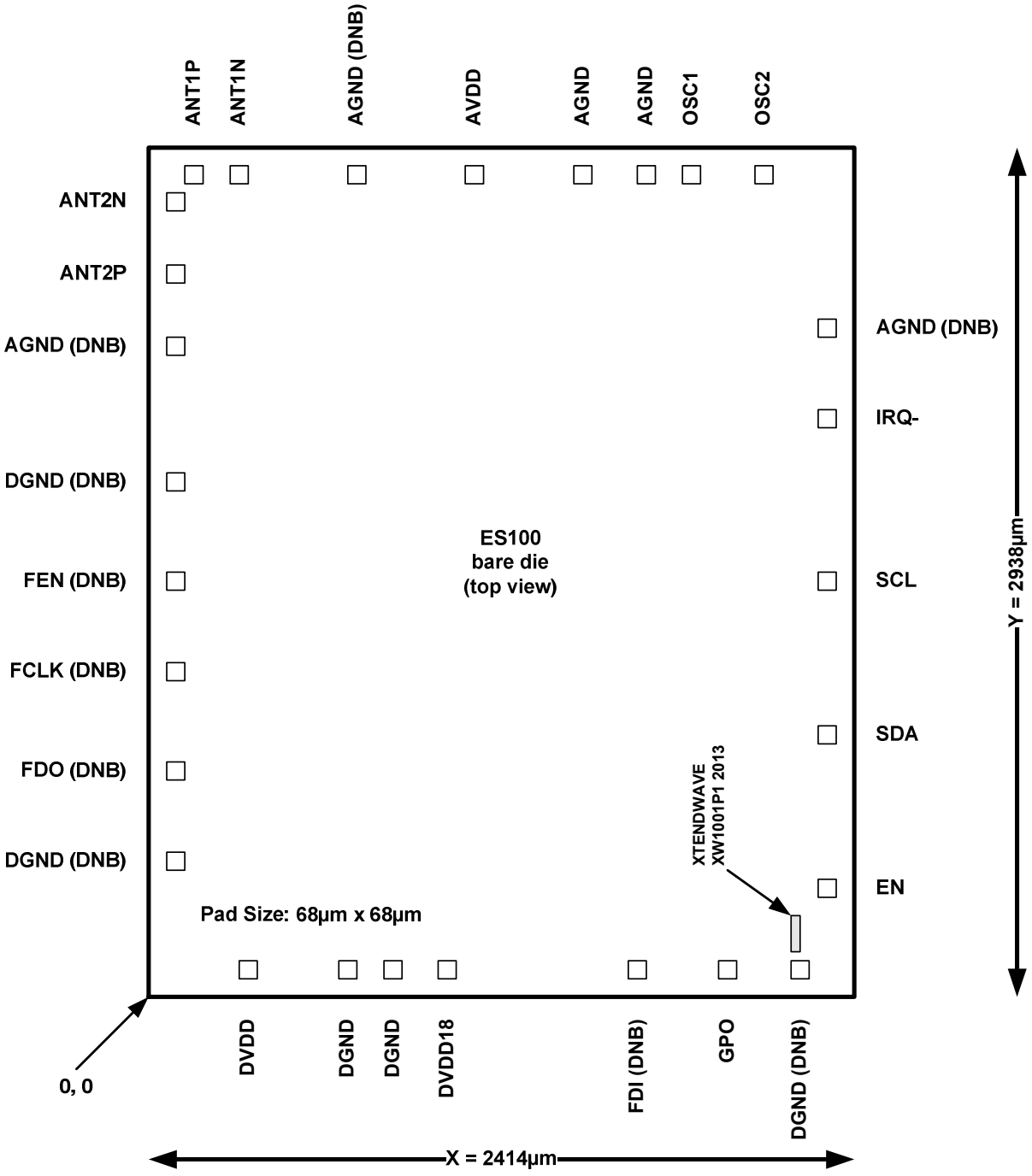
Note: Digital pins float during shutdown.

BARE DIE BOND PAD LOCATIONS

The coordinates in the table below correspond to the bond pad center points.

- Number of pads to bond: 18
- Number of un-bonded pads: 10
- Bond pad size: 68µm x 68µm

	Pad Name	coordinates [µm]		Notes
		X	Y	
1	ANT2N	90	2743	
2	ANT2P	90	2487	
3	AGND	90	2244	Do Not Bond
4	DGND	90	1781	Do Not Bond
5	FEN	90	1453	Do Not Bond
6	FCLK	90	1121	Do Not Bond
7	FDO	90	793	Do Not Bond
8	DGND	90	462	Do Not Bond
9	DVDD	352	95	
10	DGND	684	95	
11	DGND	845	95	
12	DVDD18	1045	95	
13	FDI	1674	95	Do Not Bond
14	GPO	1992	95	
15	DGND	2240	95	Do Not Bond
16	EN	2320	373	
17	SDA	2320	909	
18	SCL	2320	1430	
19	IRQ-	2320	2016	
20	AGND	2320	2313	Do Not Bond
21	OSC2	2138	2846	
22	OSC1	1871	2846	
23	AGND	1717	2846	
24	AGND	1492	2846	
25	AVDD	1098	2846	
26	AGND	712	2846	Do Not Bond
27	ANT1N	297	2846	
28	ANT1P	150	2846	



DNB: Do Not Bond

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Supply Voltage (AVDD, DVDD)	3.6V
Storage Temperature Range	-40°C to +125°C
Analog Inputs (ANT1P, ANT1N, ANT2P, ANT2N)	(GND – 0.3V) to (VDD + 0.3V)
Digital Inputs	(GND – 0.3V) to (VDD + 0.3V)
Junction Temperature	125°C
Lead Temperature (10sec)	300°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Max	Unit
Supply Input Voltage (AVDD, DVDD)	2.0	3.6	V
Operating Ambient Temperature	see ordering table on page 24		

CHARACTERISTICS

VDD = 2.0 to 3.6V and over specified ambient temperature range unless otherwise specified.
VDD = 3.3V and Ta = 25°C for typical values.

Parameter	Conditions	Min	Typ	Max	Units
ANTENNA INPUTS					
Minimum Signal Voltage	Test circuit #1		0.04		µVrms
Minimum Signal Voltage	Test circuit #2		0.1		µVrms
Maximum Signal Voltage		0.1			Vrms
Input Resistance	Differential	0.5			MΩ
Input Capacitance				10	pF
DIGITAL INPUTS					
Logic Low Voltage				0.3·VDD	V
Logic High Voltage		0.7·VDD			V
DIGITAL OUTPUTS					
Logic Low Voltage	I_{OL} = 2mA			0.2·VDD	V
Logic High Voltage	I_{OH} = 2mA	0.8·VDD			V
XOSC INPUTS					
Crystal Frequency			16		MHz
Frequency Tolerance	25°C			+/-30	ppm
Frequency Stability	Over ambient temp. range			+/-30	Ppm
Crystal ESR				100	Ω
SERIAL INTERFACE					
SCL Frequency		0		400	kHz
POWER SUPPLY					
AVDD/DVDD Range		2.0		3.6	V
Receive Current	EN = 1, START=1		8		mA
Processing Current	EN = 1, START=1		28		mA
Idle Current	EN = 1, START=0		2.5		mA
Shutdown Current	EN = 0		0.1		µA
TIMING					
Wakeup	From rising edge of IRQ-		1.0		ms
1-Minute Frame Reception	From Start command to IRQ-falling-edge.		134		s
Tracking Reception	From Start command to IRQ-falling-edge.		24.5		s
IRQ- Delay	From second boundary to IRQ-falling-edge	-100		100	ms

THEORY OF OPERATION

POWER STATES

The ES100 supports three power states: ACTIVE, IDLE and SHUTDOWN. The power states are controlled by the EN digital input and serial interface commands. The rising edge of EN triggers the transition from SHUTDOWN to IDLE and the falling edge causes a transition from any other state to SHUTDOWN. The ES100 moves between IDLE and ACTIVE power states depending on serial interface commands. This is illustrated in Figure 1.

Note that the digital pins float during shutdown. Pullup or pulldown resistors may be required.

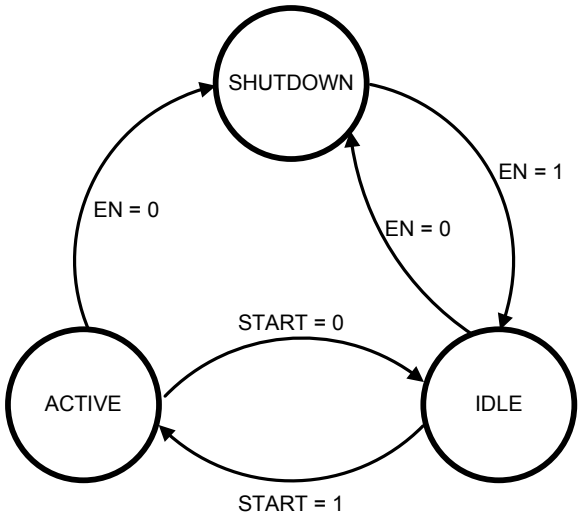


Figure 1 State Diagram: Power States

1-MINUTE FRAME RECEPTION EXAMPLE 1

Figure 2 shows the timing for a reception attempt where the time and date are successfully received on the first attempt. The rising edge on the EN pin initiates the wakeup of the receiver. After the t_{wakeup} delay, the host microcontroller initiates the reception attempt by writing to the CONTROL 0 register to set the START bit high. This will cause the ES100 to begin signal reception and processing. After receiving and processing the signal, the ES100 will generate a falling edge on the IRQ- output pin. The host microcontroller then reads the IRQ Status register to determine what caused the interrupt. If the RX_COMPLETE bit is set, as in this example, the Status, Date, Time, and Next DST registers are all valid and can be read by the host. After reading the registers, the host sets the EN pin low, returning the ES100 to shutdown mode.

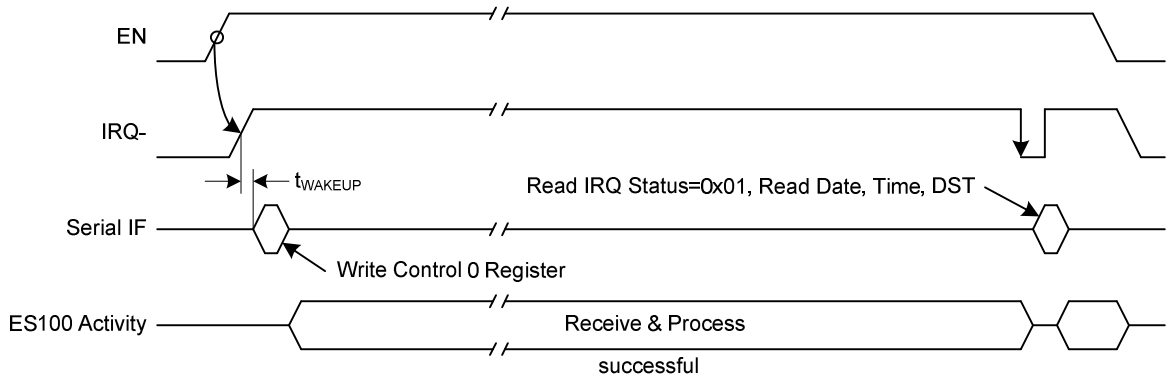


Figure 2 Timing Diagram for first attempt success

1-MINUTE FRAME RECEPTION EXAMPLE 2

Figure 3 shows the timing for a reception attempt where the time and date are successfully received on the second attempt. The rising edge on the EN pin initiates the wakeup of the receiver. After the t_{wakeup} delay, the host microcontroller initiates the reception attempt by writing to the CONTROL 0 register to set the START bit high. This will cause the ES100 to begin signal reception and processing. After receiving and processing the signal, the ES100 will generate a falling edge on the IRQ- output pin. The host microcontroller then reads the IRQ Status register to determine what caused the interrupt. When the IRQ STATUS register is read with the CYCLE COMPLETE bit set high, indicating an unsuccessful reception attempt, the ES100 automatically drives the IRQ- pin back high and attempts another reception. If the RX_COMPLETE bit is set, as in the second attempt in this example, the Status, Date, Time, and Next DST registers are all valid and can be read by the host. After reading the registers, the host sets the EN pin low, returning the ES100 to shutdown mode. If multiple unsuccessful reception attempts occur, the ES100 will automatically continue receiving and processing until terminated by the host setting EN low.

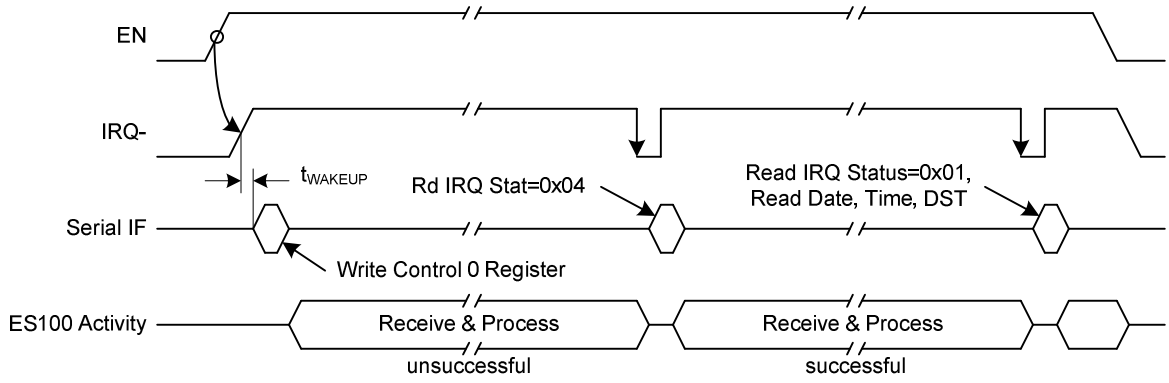


Figure 3 Timing diagram for second attempt success

Figure 4 shows the relationship between the IRQ- falling-edge, after a successful reception, and the value that is stored in the Second register (register 0x09). As shown, if the IRQ edge occurs at the boundary between second :xx+1 and second :xx+2, the register will contain second :xx+2.

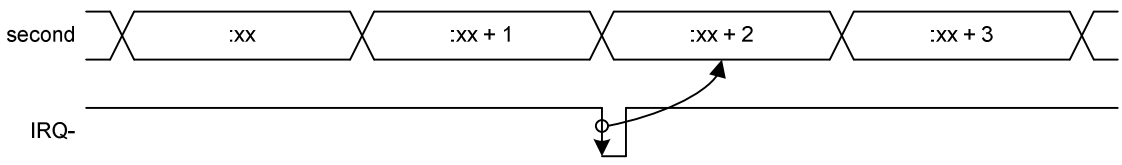


Figure 4 IRQ relationship to second register

TRACKING

The ES100 tracking operation is a reception mode targeted at periodic drift adjustments. It is based on the reception of the known 13-bit synchronization word at the beginning of each 1-minute frame, plus the "0" that is always present at second :59 preceding the sync word. This mode does not perform a complete date and time reception; it only provides the second. Consequently, the tracking operation is shorter in duration, consumes less energy, is more robust, and can be successful in lower SNR conditions than the 1-minute frame reception.

The duration of a tracking reception is ~24.5 seconds (22 seconds of reception, plus ~2.5 seconds of processing and IRQ- generation), compared to ~134 seconds for a 1-minute frame reception. A tracking reception is initiated by asserting the EN pin high and writing either 0x15 (for a one-time tracking reception using antenna 1) or 0x13 (for a one-time tracking reception using antenna 2) to the Control 0 register. The write to Control 0 must occur when the clock second transitions to :55 (refer to the timing diagrams to see how this supports drift between +4s and -4s). Tracking detects the WWVB sync word, including the leading "0" at second :59, and provides (in register 0x09) the current WWVB second that begins on the falling-edge of IRQ-. Note that the registers representing the Year, Month, Day, Hour, Minute and Next DST are not valid for a tracking reception.

The tracking operation was designed to allow for the compensation of drift that is limited to ±4 seconds. If a time drift greater than 4 seconds has been experienced before a tracking operation is initiated at second :55, the operation will fail to recover the correct timing. A failed tracking operation will typically be identified by RX_OK = 0 in the Status 0 register. However, in cases where the timing drift is considerably greater than 4 seconds, the tracking operation might report a false success due to a portion of the received data appearing similar to the sync word. Whenever the timing drift has exceeded 4 seconds in either direction, the RCC may recover the correct timing by attempting a 1-minute frame reception.

When implementing tracking reception in the host MCU, it is very important to analyze and understand the system level drift potential, and to ensure that it is within ±4 seconds relative to WWVB. The total time drift is the sum of the inherent timing error of the ES100 (the inaccuracy of the IRQ- Delay parameter in the ES100 data sheet characteristics table), and the drift associated with the host MCU crystal oscillator frequency errors (which, beyond the basic tolerance specified for the crystal, may also be affected by factors such as temperature and aging). If multiple un-successful tracking reception attempts occur over several hours, the additional drift must also be factored in. Another consideration in the drift budget, which could add or subtract 1 one full second, would be a leap second that has occurred since the previous reception, which the MCU had not accounted for. Note that advance notice of upcoming leap seconds are provided in the broadcast (LSW[1:0] in the Status 0 register), which allow the MCU to schedule an automatic 1-second timing adjustment at the correct instance.

Figure 5 shows the timing within the clock when its time has drifted +4 seconds relative to the WWVB broadcast time. Figure 6 shows the timing when the clock time has drifted -4 seconds relative to the WWVB broadcast time. The EN assertion and Control 0 register write at clock second :55 ensures that the entire WWVB sync word falls within the 22 second reception time in both extreme cases. After a tracking reception attempt, the RX_COMPLETE bit in the IRQ Status register will be set to "1" (this is true for either a success or failure of the tracking reception attempt). A successful tracking reception attempt will be indicated by both RX_OK=1 and TRACKING=1 in the Status 0 register. If either of these bits are "0", the tracking operation failed.

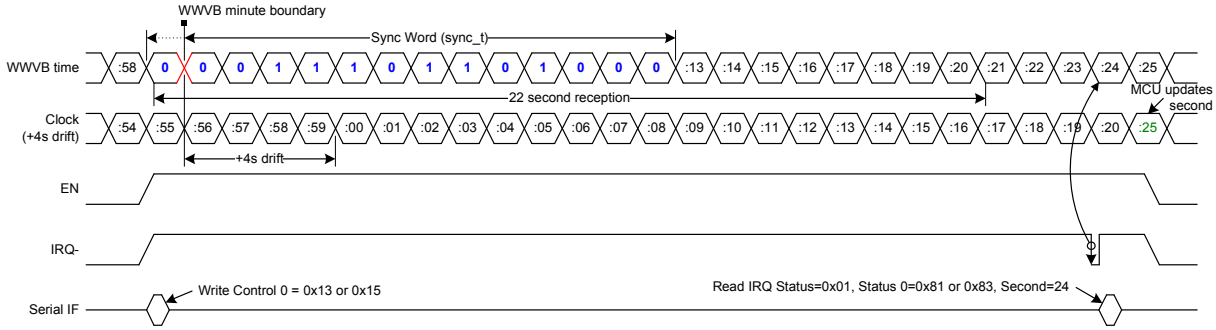


Figure 5 Clock Time has drifted +4 seconds relative to WWVB

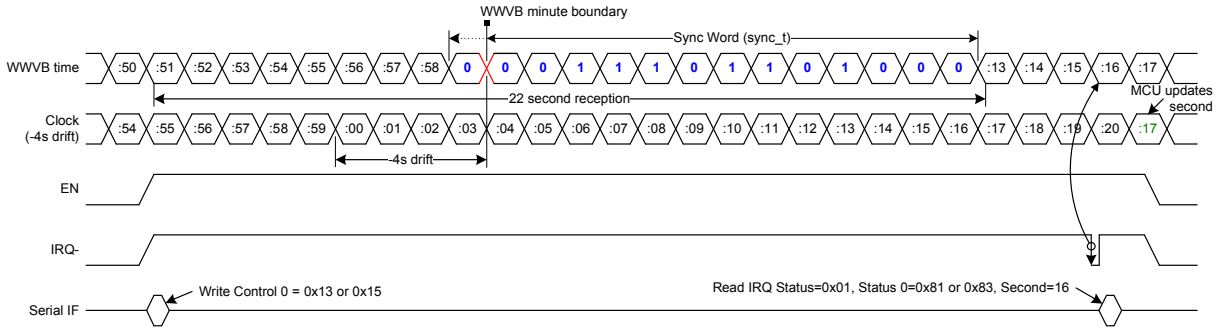


Figure 6 Clock Time has drifted -4 seconds relative to WWVB

RECEPTION CURRENT

The chart shown in Figure 7 represents the ES100 current consumption during a 1-minute frame reception. In this example, the signal receive time begins at second 5 and ends at second 126 for a total duration of 121 seconds. The signal processing time begins at second 126 and ends at second 138 for a total duration of 12 seconds. There is an additional amount of time (1 second or less) required to generate the IRQ- signal at the proper time on the 1-second boundary. The total energy consumption for the 1-minute frame reception is calculated using this equation:

$[(121s \times I_R) + (12s \times I_P) + (1s \times I_R)] \times VDD$

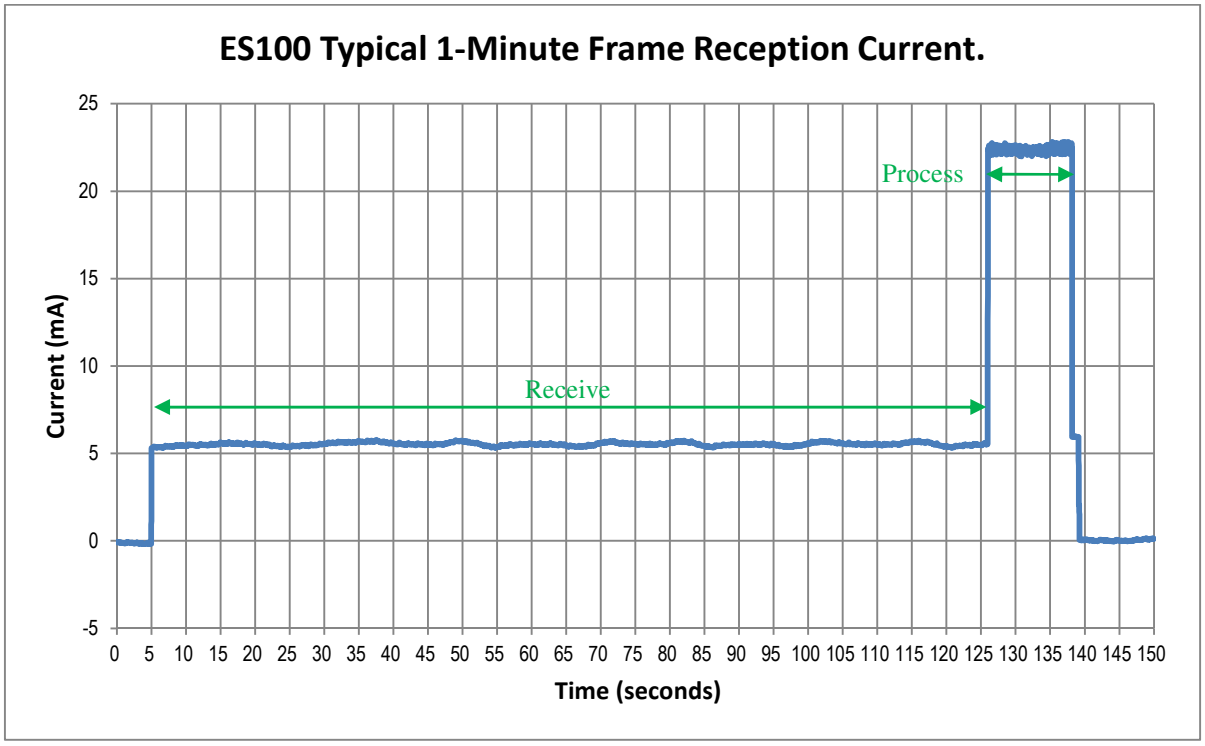


Figure 7 - ES100 1-Minute Frame Reception Current

The chart shown in Figure 8 represents the ES100 current consumption during a tracking reception. In this example, the signal receive time begins at second 4 and ends at second 26 for a total duration of 22 seconds. The signal processing time begins at second 26 and ends at second 27.5 for a total duration of 1.5 seconds. There is an additional amount of time (1 second or less) required to generate the IRQ- signal at the proper time on the 1-second boundary. The total energy consumption for the tracking reception is calculated as follows:

$[(22s \times I_R) + (1.5s \times I_P) + (1s \times I_R)] \times VDD$

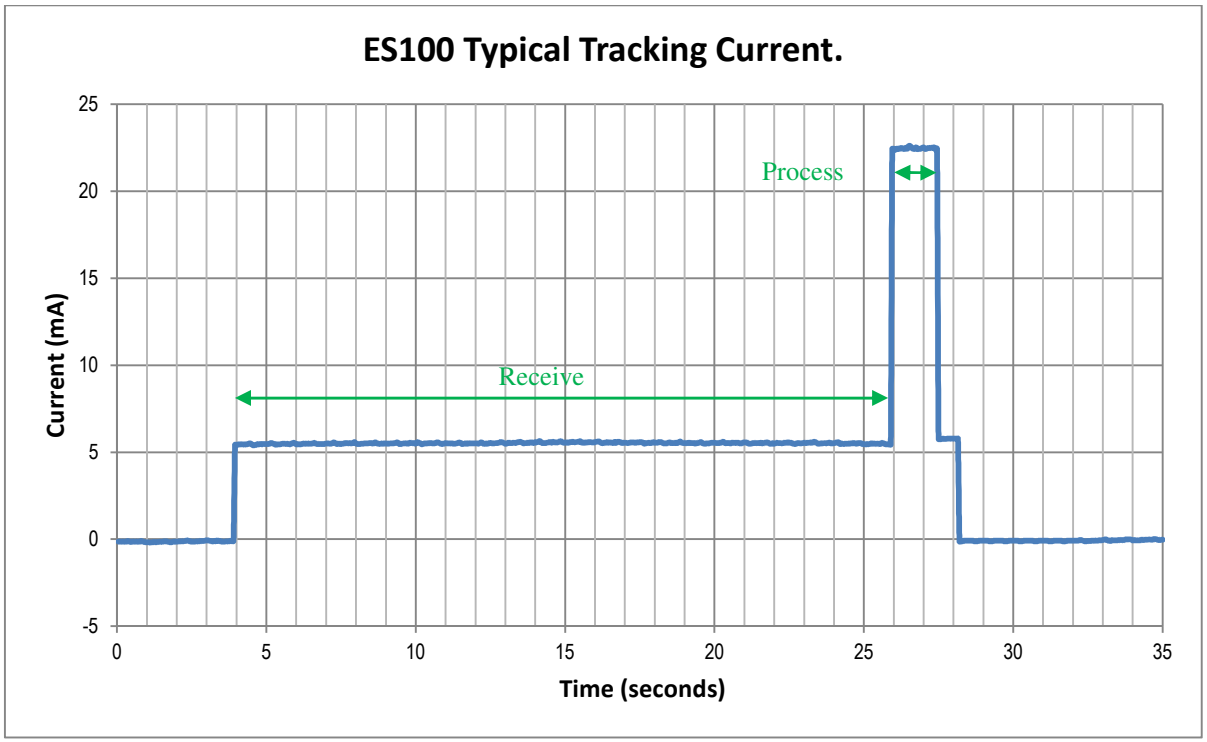


Figure 8 - ES100 Tracking Reception Current

DST_LS DECODE

The ES100 decodes the DST_LS[4:0] field that is present in the WWVB Phase Modulation broadcast. The decoded Daylight Saving Time (DST) information is available in the Status 0 register (bits 6:5) and the decoded Leap Second (LS) information is available in the Status 0 register (bits 4:3). These two pairs of bits define the state of DST and LS at the time of reception. The DST information should be applied when the clock time is set. The LS information applies to the current month and may be used to add or subtract one second during the final minute of the current month. The tables below describe the decoded bits.

DST[1:0]	Description
00	DST is not in effect.
10	DST begins today. At the appropriate local time, set the clock ahead 1 hour.
11	DST is in effect.
01	DST ends today. At the appropriate local time, set the clock back 1 hour.

LS[1:0]	Description
0x	There is not a leap second in the current month
10	There is a negative leap second in the current month. If desired, delete one second from the final minute of the month.
11	There is a positive leap second in the current month. If desired, add one second to the final minute of the month.

DST_NEXT DECODE

The ES100 decodes the DST_NEXT[5:0] field that is present in the WWVB Phase Modulation broadcast. The decoded Next Daylight Saving Time (DST) information provides advanced notice of the month, day and local time for the upcoming DST transition. This information is available for the host MCU to read in the Next DST Month register, the Next DST Day register, and the Next DST Hour register. The Next DST information can be read months in advance of the actual transition, stored by the host MCU, and applied on the appropriate day.

APPLICATION CIRCUIT

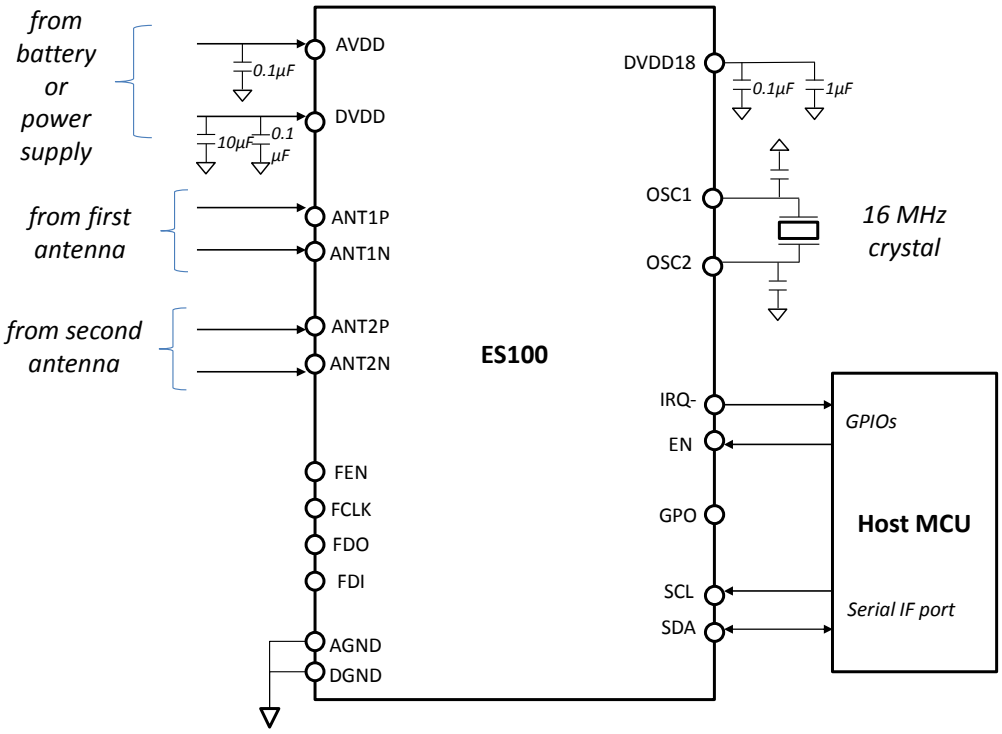


Figure 9 Application Diagram

SUGGESTED CRYSTAL SUPPLIERS

Supplier	Part Number	Load capacitor
NDK	NX5032GC-16MHZ-STD-CSK-6	16pF, 1%, COG(NPO)
CTS	TS160F33CCT	32 pF, 1%, COG(NPO)
ECS	ECS-160-16-5PX-GM-TR-815	32 pF, 1%, COG(NPO)

Note: Capacitor values may need to be adjusted due to PCB parasitic capacitance.

SERIAL INTERFACE REGISTER MAP

Addr	Description	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	Control 0	RW	0	0	0	TRACKING ENABLE	START ANTENNA	ANT2 OFF	ANT1 OFF	START
0x01	Control 1	RW	0	0	0	0	0	0	0	0
0x02	IRQ Status	R	0	0	0	0	0	CYCLE COMPLETE	RSVD	RX_COMPLETE
0x03	Status 0	R	TRACKING	DST1	DST0	LSW1	LSW0	RSVD	ANT	RX_OK
0x04	Year	R	10 Year				Year			
0x05	Month	R	0	0	0	10Month	Month			
0x06	Day	R	0	0	10Day		Day			
0x07	Hour	R	0	0	10Hour		Hour			
0x08	Minute	R	0	10Minute			Minute			
0x09	Second	R	0	10Second			Second			
0x0A	Next DST Month	R	0	0	0	DST10Month	DSTMonth			
0x0B	Next DST Day	R	0	0	DST10Day		DSTDay			
0x0C	Next DST Hour	R	DSTSpecial				DSTHour			
0x0D	Device ID	R	DeviceID							
0x0E	reserved	R	0	0	0	0	0	0	0	0
0x0F	reserved	R	0	0	0	0	0	0	0	0

REGISTER DESCRIPTIONS

Control 0:

Name: Control 0			Address: 0x00			Type: R/W	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	TRACKING ENABLE	START ANTENNA	ANT2 OFF	ANT1 OFF	START

START	Description
1	When the START bit is written with a 1, the status, date, and time registers are all cleared, bits 4:1 are sampled, and the ES100 begins receiving and processing the input signal.
0	ES100 stops receiving and processing the input signal. This will automatically occur at the end of a successful reception. It can be forced to occur by the host processor writing a 0. (default)

ANT1 OFF	Description
1	Antenna 1 input disabled.
0	Antenna 1 input enabled. (default)

ANT2 OFF	Description
1	Antenna 2 input disabled.
0	Antenna 2 input enabled. (default)

START ANTENNA	Description
1	Start reception with antenna 2.
0	Start reception with antenna 1. (default)

TRACKING ENABLE	Description
1	Tracking mode enabled.
0	Tracking mode disabled. (default)

Notes for Control 0 Register:

- Bits 5-7 must always be written with 0.

Valid Control 0 Register Write Values	
Value	**Description**
0x01	Normal 1-minute frame reception. Starts with Antenna 1. Toggles between Antenna 1 and Antenna 2. Continues reception attempts until successful, or stopped by host MCU.
0x03	1-minute frame reception using Antenna 2 only. Continues reception attempts until successful, or stopped by host MCU.
0x05	1-minute frame reception using Antenna 1 only. Continues reception attempts until successful, or stopped by host MCU.
0x09	Normal 1-minute frame reception. Starts with Antenna 2. Toggles between Antenna 2 and Antenna 1. Continues reception attempts until successful, or stopped by host MCU.
0x13	Tracking reception attempt using Antenna 2. Single reception attempt. Must be properly timed in order to acquire the Sync Word.
0x15	Tracking reception attempt using Antenna 1. Single reception attempt. Must be properly timed in order to acquire the Sync Word.

Control 1:

Name: Control 1			Address: 0x01			Type: R/W	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	0	0	0	0	0

The Control 1 Register is currently unused.

IRQ Status:

Name: IRQ Status			Address: 0x02			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	0	0	CYCLE COMPLETE	RESERVED	RX_COMP

RX_COMP	Description
1	Reception Complete. Indicates that IRQ- went active due to a successful reception.
0	(default)

RESERVED	Description
1	
0	(default)

CYCLE COMPLETE	Description
1	Cycle Complete. Indicates that IRQ- went active due to the unsuccessful completion of a reception attempt.
0	(default)

Notes for IRQ Status Register:

- Reading the IRQ Status register causes the IRQ- signal to go high.

Status 0:

Name: Status 0			Address: 0x03			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
TRACKING	DST1	DST0	LSW1	LSW0	RSVD	ANT	RX_OK

RX_OK	Description
1	Indicates that a successful reception has occurred.
0	Indicates that a successful reception has not occurred.

ANT	Description
1	Indicates that the reception occurred on Antenna 2.
0	Indicates that the reception occurred on Antenna 1.

RSVD	Description
1	Reserved.
0	Reserved. (default)

LSW[1:0]	Description
0x	Indicates that the current month will not have a leap second.
10	Indicates that the current month will have a negative leap second.
11	Indicates that the current month will have a positive leap second.

DST[1:0]	Description
00	Indicates that Daylight Savings Time (DST) is not in effect.
10	Indicates that DST begins today.
11	Indicates that DST is in effect.
01	Indicates that DST ends today.

TRACKING	Description
1	Indicates that the reception attempt was a tracking operation.
0	Indicates that the reception attempt was a 1-minute frame operation.

Notes for Status 0 Register:

- Bits 1-7 are only valid if bit 0 = 1.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- LSW[1:0] and DST[1:0] are decoded from DST_LS[4:0] in the WWVB-PM data stream.

Year:

Name: Year			Address: 0x04			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
10Year[3:0]				Year[3:0]			

Year[3:0]	Description
	This is a Binary Coded Decimal (BCD) representation of the first digit of the received year.

10Year[3:0]	Description
	This is a BCD representation of the second digit of the received year.

Notes for Year Register:

- Year register contents are only valid if RX_OK = 1 in the Status 0 register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- Example: the year 2049 is represented by 01001001b.

Month:

Name: Month			Address: 0x05			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	10Month	Month[3:0]			

Month[3:0]	Description
	This is a BCD representation of the first digit of the received month.

10Month	Description
	This is a BCD representation of the second digit of the received month.

Notes for Month Register:

- Month register contents are only valid if RX_OK = 1 in the Status 0 register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- Example: November is represented by 00010001b.

Day:

Name: Day			Address: 0x06			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	10Day[1:0]		Day[3:0]			

Day[3:0]	Description
	This is a BCD representation of the first digit of the received day of the month.

10Day[1:0]	Description
	This is a BCD representation of the second digit of the received day of the month.

Notes for Day Register:

- Day register contents are only valid if RX_OK = 1 in the Status 0 register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- Example: The 26th is represented by 00100110b.

Hour:

Name: Hour			Address: 0x07			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	10Hour[1:0]		Hour[3:0]			

Hour[3:0]	Description
	This is a BCD representation of the first digit of the received UTC hour.

10Hour[1:0]	Description
	This is a BCD representation of the second digit of the received UTC hour.

Notes for Hour Register:

- Hour register contents are only valid if RX_OK = 1 in the Status 0 register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- Example: The 23rd hour is represented by 00100011b.

Minute:

Name: Minute			Address: 0x08			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	10Minute[2:0]			Minute[3:0]			

Minute[3:0]	Description
	This is a BCD representation of the first digit of the received minute.

10Minute[2:0]	Description
	This is a BCD representation of the second digit of the received minute.

Notes for Minute Register:

- Minute register contents are only valid if RX_OK = 1 in the Status 0 register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- Example: The 57th minute is represented by 01010111b.

Second:

Name: Second			Address: 0x09			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	10Second[1:0]			Second[3:0]			

Second[3:0]	Description
	This is a BCD representation of the first digit of the received second.

10Second[2:0]	Description
	This is a BCD representation of the second digit of the received second.

Notes for Second Register:

- Second register contents are only valid if RX_OK = 1 in the Status 0 register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- Example: The 48th second is represented by 01001000b.

Next DST Month:

Name: Next DST Month			Address: 0x0A			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	DST10Month	DSTMonth[3:0]			

DSTMonth[3:0]	Description
	This is a BCD representation of the first digit of the month of the next DST transition.

DST10Month	Description
	This is a BCD representation of the second digit of the month of the next DST transition.

Notes for Next DST Month Register:

- Month register contents are only valid if RX_OK = 1 in the Status 0 register and DSTSpecial[3] = 0 in the Next DST Hour register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- The month is decoded from DST_NEXT[5:0] in the WWVB-PM data stream.

Next DST Day:

Name: Next DST Day			Address: 0x0B			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	DST10Day[1:0]		DSTDay[3:0]			

DSTDay[3:0]	Description
	This is a BCD representation of the first digit of the day of the next DST transition.

DST10Day[1:0]	Description
	This is a BCD representation of the second digit of the day of the next DST transition.

Notes for Next DST Day Register:

- Day register contents are only valid if RX_OK = 1 in the Status 0 register and DSTSpecial[3] = 0 in the Next DST Hour register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- The day is decoded from DST_NEXT[5:0] in the WWVB-PM data stream.

Next DST Hour:

Name: Next DST Hour			Address: 0x0C			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DSTSpecial[3:0]				DSTHour[3:0]			

DSTHour[3:0]	Description
	This is a BCD representation of the UTC hour of the next DST transition.

DSTSpecial[3:0]	Description
0xxx	No DST Special condition. (Next DST Month, Next DST Day and Next DST Hour fields are valid.)
1000	DST date and time is outside of defined schedule table
1001	DST off (regardless of date)
1010	DST on (regardless of date)
1011	Reserved 1
1100	Reserved 2
1101	Reserved 3
1110	Reserved 4
1111	Reserved 5

Notes for Next DST Hour Register:

- Next DST Hour[3:0] contents are only valid if DSTSpecial[3] = 0 and RX_OK = 1 in the Status 0 register.
- All bits are cleared when the START bit in the CONTROL 0 register is written with a 1.
- The hour/special condition is decoded from DST_NEXT[5:0] in the WWVB-PM data stream.
- Valid Next DST Hours are 1am, 2am, 3am.

Device ID:

Name: Device ID			Address: 0x0D			Type: R	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DeviceID[7:0]							

DeviceID[7:0]	Description
0x10	Device ID = ES100

SERIAL INTERFACE OPERATION

The serial interface consists of the bi-directional serial data signal (SDA) and the serial clock input signal (SCL). The ES100 operates as a slave device only. The slave address is 0x32. Serial interface write and read transaction timing is shown in Figures 11, 12 and 13. The interface supports single byte writes, single byte reads, and multi byte reads. For multi byte reads, the register address increments after each data byte is read.

Important: The ES100 should be placed on a dedicated serial interface so that reception is not compromised by serial interface traffic directed at another device.

The AC characteristics of the serial interface are shown in the table below and in Figure 10.

Guaranteed by initial characterization.

Parameter	Symbol	Std Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100		400	kHz
LOW period of SCL	t_{LOW}	4.7		1.3		µs
HIGH period of SCL	t_{HIGH}	4.0		0.6		µs
Rise time (SDA & SCL)	t_R		1000		300	ns
Fall time (SDA & SCL)	t_F		300		300	ns
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7		0.6		µs
START condition hold time	$t_{HD;STA}$	4.0		0.6		µs
Data set-up time	$t_{SU;DAT}$	250		100		ns
Data hold time	$t_{HD;DAT}$	0		0		µs
Set-up time for STOP condition	$t_{SU;STO}$	4.0		0.6		µs
Bus free time between STOP and START condition	t_{BUF}	4.7		1.3		µs

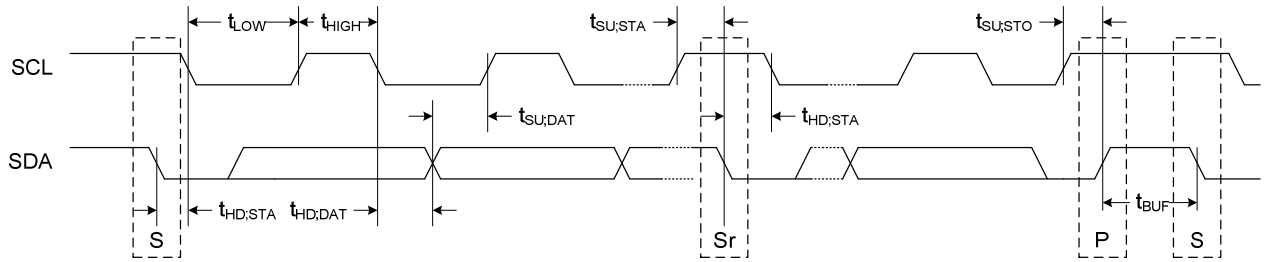


Figure 10 Serial Interface Timing

SERIAL INTERFACE WAVEFORMS

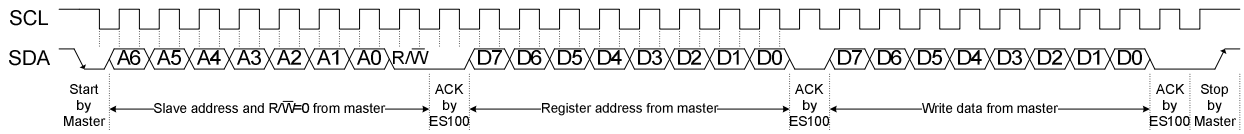


Figure 11 Serial Interface Single Byte Write

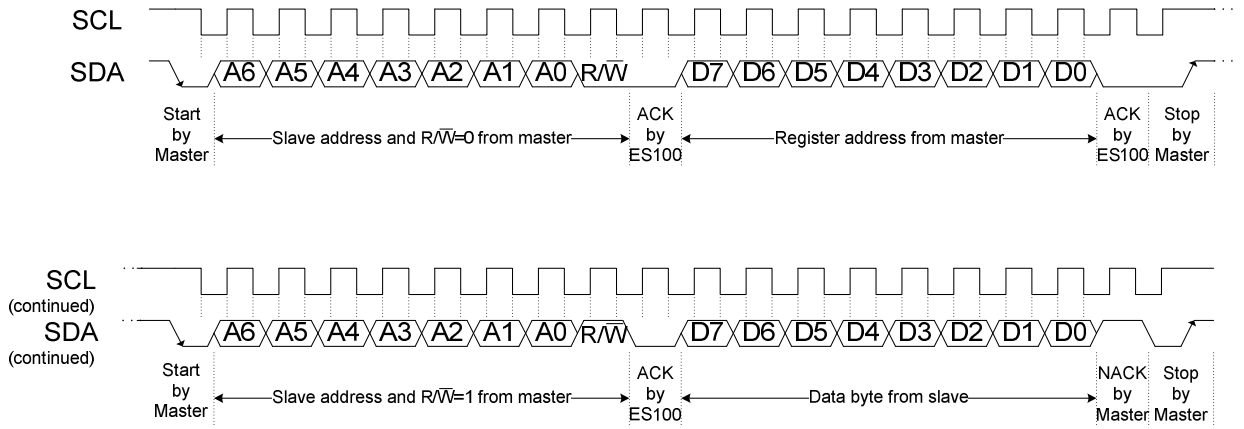


Figure 12 Serial Interface Single Byte Read

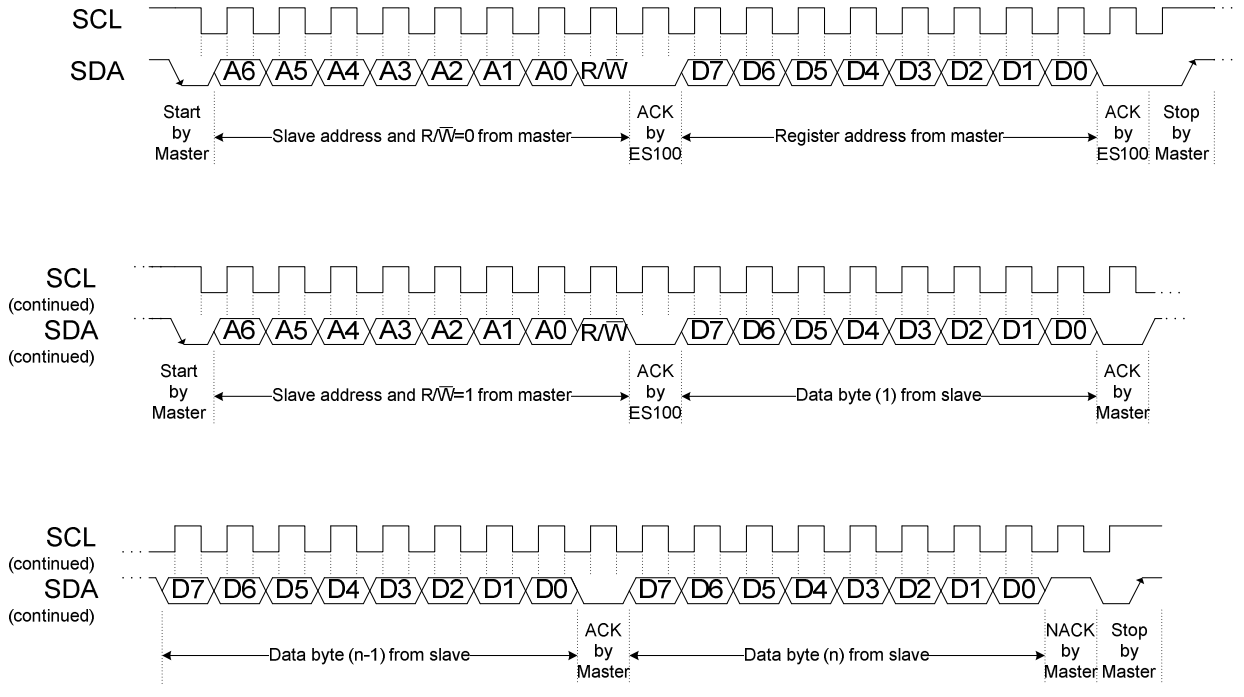


Figure 13 Serial Interface Multi Byte Read

PCB LAYOUT CONSIDERATIONS

- Place crystal and load capacitors as close as possible to pins OSC1 and OSC2. Route traces symmetrically.
- Route antenna input trace pairs so there is some separation/isolation between them.
- Place 0.1 µF and 10 µF capacitors as close as possible to the DVDD pin.
- Place 0.1 µF and 1 µF capacitors as close as possible to the DVDD18 pin.
- Place 0.1 µF capacitor as close as possible to the AVDD pin.

SELF-INTERFERENCE MINIMIZATION

The recommendations in this section are intended to minimize the potential for self-induced interference that could degrade receiver sensitivity. Various potential sources of interferences, including power/ground and digital signals, may cause electromagnetic interference (EMI) that could couple into the antennas. To minimize the potential for EMI, the design of the system incorporating the receiver, as well as the design of the printed circuit board and the wiring around it, must consider the following guidelines:

- If wires are used to carry power from a battery pack or from whatever other source, they should be twisted to minimize the potential for EMI created by loops in the wiring.
- If power is fed through PCB routing, the power and ground leading to a particular load should be placed tightly together, to minimize the area of potential loops. Note that the characteristics of the current consumed by many loads, such as the ES100 IC itself, may contain noise that could potentially create EMI.
- The use of wire-wound inductors (such as dc-filtering chokes), through which time-varying currents may flow, should be avoided.
- Avoid any clock frequencies or periodic operations that could generate a harmonic at 60 kHz, the center frequency of the receiver.
- Place antennas as far as possible from sources of interference that may be active during reception.

ORDERING INFO

Part Number	Temperature	Package	Order Multiple
ES100C-B	-10 to +70℃	Bare Die	150
ES100I-B	-40 to +85℃	Bare Die	150

TEST CIRCUITS

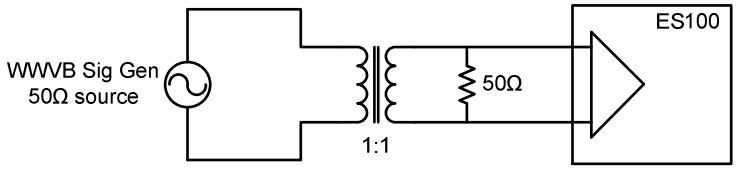


Figure 14 Test Circuit #1

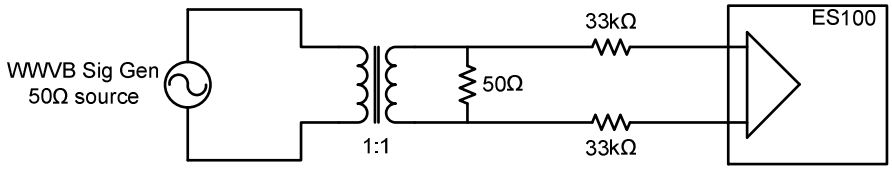


Figure 15 Test Circuit #2